Amendment to the Specification

Please amend the specification as follows:

[0028] Figure 7 illustrates the architecture of a system of the present invention. Ingress ports 1 through N, one of which is labelled as **110**, receive data grains ordered as grain groups. Preferably the grains are received synchronously across the number of ingress ports. From ingress ports **110**, the grains are aggregated by aggregator **202** into an N grain wide channel **203**. For the purposes of this exemplary illustration, each data grain is assumed to be 1 byte in size, resulting in a requirement for an N byte wide channel to correspond to the N ingress ports. The N byte word representing the received grains is provided to the memory egress self selection (MESS) egress ports, one of which is labelled **204**. Each MESS port **204** stores only the grains that it will transmit in an internal memory. Because each MESS port **204** has its own internal memory, the complex multiplexing circuitry utilized by the flip-flop based implementation is eliminated in favor of the simplified multiplexing circuitry of the RAM based implementation previously described. However, MESS port **204** is provided with processing capacity to determine which data grains are of interest, that is, which received data grains will be transmitted over the particular MESS port **204**. By discarding the grains of no interest, or conversely by selecting the grains of interest, only the selected grains need to be stored which reduces the required memory storage for each port.

[0029] Figure 8 provides a more detailed architecture for a system of the present invention. Data grains are received by ingress ports, aggregated into an N byte wide channel **203**, and ~~one of which is labelled as **110**. The grains received by the ingress ports are~~ provided to ingress processor **206** in MESS egress port **204**. Ingress processor **206** selects data grains ~~from the ingress ports **110**~~ for storage in memory **208**. Whereas the RAM based implementation required N RAMs of G bytes, the present invention reduces the required RAM, as only the grains to be transmitted by the egress port are stored. As a statistical average, this means that each of the N memories can be reduced in size to G/N from G. Over N ingress and egress ports, this reduces the memory size to G bytes from an original GN bytes. To multiplex out the stored grains while new grains are received, a double buffering implementation can be employed. The order of the addresses to be read out from the memory is provided by an egress processor **212** which accesses connection memory **214**. The reading

of the stored grains uses a simple N:1 multiplexer **210** on a per port basis. This combines the reduced memory requirement advantage of the standard flip-flop implementation with the simplified multiplexing circuitry advantage of the RAM implementation.